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2	19740	(copper and stress) and (interconnect\$ or wiring)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/11 09:58
3	10853	((copper and stress) and (interconnect\$ or wiring)) and semiconductor	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/11 09:58
4	9730	((((copper and stress) and (interconnect\$ or wiring)) and semiconductor) and (hole or via or opening or slit or slot))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/11 10:00
5	7056	(((((copper and stress) and (interconnect\$ or wiring)) and semiconductor) and (hole or via or opening or slit or slot)) and etch\$	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/11 10:00
6	5413	((((((copper and stress) and (interconnect\$ or wiring)) and semiconductor) and (hole or via or opening or slit or slot)) and etch\$) and via	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/11 10:02
7	1202	((((((((copper and stress) and (interconnect\$ or wiring)) and semiconductor) and (hole or via or opening or slit or slot)) and etch\$) and via) and (relief or migrat\$)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/11 10:54
8	1845	copper and (stress adj relief)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/11 10:55
9	633	(copper and (stress adj relief)) and etch\$	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/11 10:56

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- ☐ Classification codes A: Physics, 7
- ☐ Classification codes A: Physics, 8
- ☐ Classification codes A: Physics, 9
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31 **Via electromigration performance of Ti/W/Al-Cu(2%) multilayered metallization**

Martin, C.A.; McPherson, J.W.;

VLSI Multilevel Interconnection Conference, 1989. Proceedings., Sixth International IEEE, 12-13 June 1989

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32 **A double metal process: using a TiW/Mo sandwich as the first layer metal**

Hawley, F.; Levi, A.; Vasche, G.; Caywood, J.M.; Houck, B.; Boyce, J.; Tso, L.

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33 **Studies on a novel flip-chip interconnect structure. Pillar bump**

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34 **Displacement transducer using impedance variations due to core torsion**

Garshelis, I.;

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35 Finite element simulation of a nondestructive shear test for TAB bo
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38 Comparison of isothermal wafer-level EM and package-level EM for
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